Notice of Allowability	Application No.	Applicant(s)	
	10/517,766	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Jason M. Mandeville	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10 August 2007*.

2. ☒ The allowed claim(s) is/are *1 and 4-8 (now renumbered 1-6)*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10 August 2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Wan-Ching Y. Montfort on 30 August 2007.

The application has been amended as follows:

2. Amended **Claim 1** now reads:

1. An active matrix type liquid crystal display device comprising:

pixel electrodes that are arranged in a matrix and that are driven by pixel transistors respectively;

a plurality of gate lines that are connected, in a column-by-column fashion, to gate electrodes of the pixel transistors;

a plurality of source lines that are connected, in a row-by-row fashion, to source electrodes of the pixel transistors;

a gate driver that, sequentially during one selection period after another, connects one of the gate lines after another to an output point of a selection voltage feed circuit; and

a source driver that feeds an image signal to the source lines,

wherein the selection voltage feed circuit has:

a first power source for feeding a predetermined selection voltage;

a diode; and

a switch,

wherein the switch is provided between the first power source and the output point of the selection voltage feed circuit, and the diode has an anode thereof connected to [[the]] a second power source and having a cathode thereof connected between the output point of the selection voltage feed circuit and the switch, and

wherein the switch being kept on from a start of the selection period for a time span shorter than the selection period.

3. Amended **Claim 4** now reads:

4. The active matrix type liquid crystal display device of claim 1[[.]],

wherein the pixel transistors are formed of amorphous silicon.

Allowable Subject Matter

4. **Claims 1 and 4-8 (now renumbered 1-6)** are allowed.

5. The following is an examiner's statement of reasons for allowance as pertaining to **Claims 1 and 4-7**: None of the references used, either singularly or in combination, teach or fairly suggest an active matrix type liquid crystal display device comprising a selection voltage feed circuit that has a first power source for feeding a predetermined selection voltage; a diode; and a switch; wherein the switch is provided between the first power source and the output point of the selection voltage feed circuit, and the diode has an anode thereof connected to a second power source and having a cathode thereof connected between the output point of the selection voltage feed circuit and the switch, and wherein the switch being kept on from a start of a selection period for a time shorter than the selection period. Lee (7,002,542) teaches (see Fig. 4, Fig. 12 and Fig. 13) an active matrix type liquid crystal display device comprising a selection voltage feed circuit (42; see Fig. 12) that has a first power source (VDD1) for feeding a predetermined selection voltage (i.e., VDD1); and a switch (60); wherein the switch (60) is provided between a first power source (VDD1), a second power source (VDD2), and the output point of the selection voltage feed circuit (SVL), wherein the switch is kept on from a start of a selection period (i.e., the start of a horizontal synchronous interval) for a time shorter than the selection period (see Fig. 13). However, Lee does not disclose a diode that has an anode connected to the second power source and having a cathode

connected between the output point of the selection voltage feed circuit and the switch. Further, none of the references used, either singularly or in combination, teach or fairly suggest using a diode connected in the manner claimed by the applicant.

In addition, while Lee does disclose a plurality of switches (38; see Fig. 4), provided one for each gate line, these switches (38) are utilized to switch between a low-level gate voltage (Vgl; see Fig. 13) and a high-level gate voltage (Vgh), not between two stages of the high-level gate voltage (Vgh) in a single selection period as is claimed by the applicant. The switch disclosed by Lee for this purpose is the switch (60) of Fig. 12, which is not disclosed or suggested to be a plurality switches provided one for each gate line. As such, the plurality of switches (38) disclosed by Lee are not an equivalent or obvious representation of the plurality of switches claimed by the applicant. None of the references used, either singularly or in combination, teach or fairly suggest using, as the switch, a plurality of switches provided one for each gate line, in parallel with one another.

6. The following is an examiner's statement of reasons for allowance as pertaining to **Claim 8**: None of the references used, either singularly or in combination, teach or fairly suggest an active matrix type liquid crystal display device comprising a selection voltage feed circuit that has a first power source for feeding a predetermined selection voltage; a second power source for feeding a voltage lower than the predetermined selection voltage; and a switch provided that so operates that, during a time span that starts at a beginning of every selection period and lasts shorter than the selection

period, the output point of the selection voltage feed circuit is fed with the voltage from the first power source; and wherein during a time span that within the selection period and during which the voltage from the first power source is not fed to the output point of the selection voltage feed circuit, the voltage from the second power source is fed to the output point of the selection voltage feed circuit; and wherein as the switch, a plurality of switches are provided one for each gate line in parallel with one another.

Again, Lee (7,002,542) teaches (see Fig. 4, Fig. 12 and Fig. 13) an active matrix type liquid crystal display device comprising a selection voltage feed circuit (42; see Fig. 12) that has a first power source (VDD1) for feeding a predetermined selection voltage (i.e., VDD1); a second power source (VDD2) for feeding a voltage lower than the predetermined selection voltage (see Fig. 13); and a switch (60) provided that so operates that, during a time span that starts at a beginning of every selection period (i.e., horizontal synchronous interval) and lasts shorter than the selection period, the output point (SVL) of the selection voltage feed circuit (42) is fed with the voltage from the first power source (VDD1); and wherein during a time span that within the selection period (i.e., horizontal synchronous interval) and during which the voltage from the first power source (VDD1) is not fed to the output point (SVL) of the selection voltage feed circuit (42), the voltage from the second power source (VDD2) is fed to the output point (SVL) of the selection voltage feed circuit (42). However, Lee does not teach or suggest that the switch (60) can be represented as a plurality of switches provided one for each gate line in parallel with one another. None of the references used, either singularly or in combination, teach or fairly suggest using, as the switch, a plurality of

switches provided one for each gate line, in parallel with one another used in the manner claimed by the applicant.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Mandeville whose telephone number is 571-270-3136. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason Mandeville
Examiner
30 August 2007

JMM

ALEXANDER EISEN
SUPERVISORY PATENT EXAMINER